

X86 Specification

*** A Community Effort ***

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X86 Specification Purposes

We believe that developing a formal instruction-set architecture (ISA) specification for the X86 architecture could serve a number of purposes.

- Documentation to be shared by hardware designers and software developers.
- Formal verification of RTL designs.
- Testing of RTL designs through "co-simulation".
- Simulation for the purpose of testing software.
- Formal verification of X86 software.

X86 Specification Elements

We believe that such a model should provide a means to specify a multiprocessor configuration, so it will be necessary to evolve a "memory centric" specification that permits interleaved execution. Each copy of an ISA processor specification, whether virtual (as in the case of hyper-threading) or physical (such as with multi-core implementations), must include its own register file, user/supervisor state, interrupt controller, and memory management unit.

Instead of attempting to take on the whole thing, I suggest we attack the specification in pieces:

- Memory system, and the memory interleaving permitted.
- Processor state.
- Various processor modes.
- Integer instructions.
- Media instructions.
- Floating-point instructions.
- Supervisor-only instructions.
- Memory management mechanisms.
- Interrupt controller.
- Virtualization mechanisms.

X86 Specification Interested Parties

There are a number of people interested in having a formal X86 specification.

- AMD – Bill, Bevier, David Russinoff
- Centaur – Terry Parks
- Intel – Everyone and noone
- Microsoft – Ernie Cohen, Yuan Yu
- Government – COTS basis for code proofs